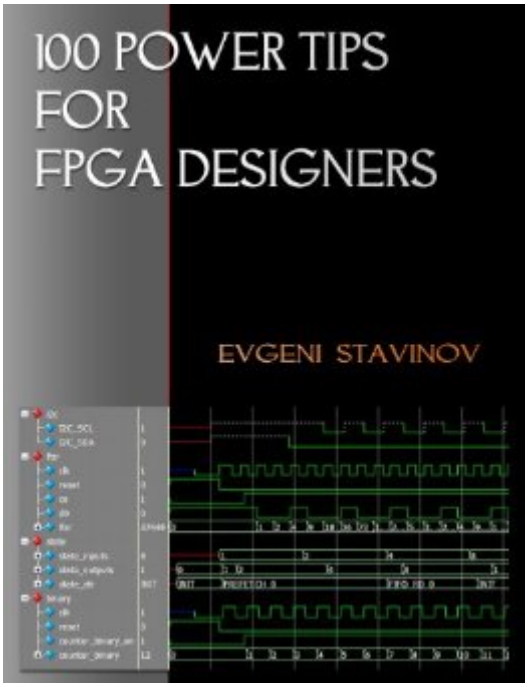
100 Power Tips For FPGA Designers



Synopsis

This book is a collection of short articles on various aspects of FPGA design: synthesis, simulation, porting ASIC designs, floorplanning and timing closure, design methodologies, performance, area and power optimizations, RTL coding, IP core selection, and many others. The book is intended for system architects, design engineers, and students who want to improve their FPGA design skills. Both novice and seasoned logic and hardware engineers can find bits of useful information.This book is written by a practicing FPGA logic designer, and contains a lot of illustrations, code examples, and scripts. Rather than providing information applicable to all FPGA vendors, this book edition focuses on Xilinx Virtex-6 and Spartan-6 FPGA families. Code examples are written in Verilog HDL. All code examples, scripts, and projects provided in the book are available on accompanying website.

Book Information

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Customer Reviews

As stated on the back cover, the book is a collection of short articles on various aspects of FPGA design. The book focuses almost exclusively on Xilinx Vertex-6 FPGAs programmed in Verilog, with some mention of the Spartan-6 line.There is no doubt that documentation is needed so designers can learn quickly how to use FPGAs effectively. The vendor documentation (from both Xilinx and Altera) is excellent but so extensive as to be overwhelming. A designer may not know where to start, and may not know the design tricks that will save them a lot of trouble. So, a need exists.Unfortunately, this book does not really fill that need. The fundamental shortcoming of the book is that the articles are overwhelmingly empty of information. To pick some examples at random:Article 25 is "Counters". The article shows Verilog for several counter architectures (binary synchronous, Johnson, LFSR, and cascaded binary synchronous counters). A table lists resource consumption and maximum counting frequency for several implementations, apparently from the Xilinx synthesis tool on the counters alone. The table includes a counter based on a Xilinx multiply-accumulate block, with only a note that the counter is included. There just doesn’t seem to be any need for this article, someone designing FPGA logic without knowing how to write a counter is not going to be rescued by this book.Article 40 is "Estimating FPGA power consumption". The article has a short paragraph on each of 3 Xilinx tools for power estimation, huge screenshots, and results from using two of the tools to estimate power for a memory controller. The tool results show an almost 2:1 difference in estimated power (1.4W vs. 2.6W), accounted for by a more than 3:1 difference in estimated I/O power consumption.

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